# NEWS AND NOTICES

The News and Notices in this issue include reprints from recent journals. The following is a list of the items included in this section.

## RECENT JOURNAL ARTICLES

- 1. <u>COMPUTER DESIGN</u> "Small Computer Features Extensive Software and File-Oriented DOS"
- 2. <u>COMPUTER DESIGN</u> 'Microcomputer Programmable ROMs''
- 3. <u>COMPUTER DESIGN</u> "Microprogrammable Computer/Controller Designed for Dedicated Applications"
- 4. DATA PRODUCT NEWS "Low-Cost Commercial Minicomputer"
- 5. <u>BENDIX TECHNICAL JOURNAL</u> "Minicomputers in Automatic Test Systems"
- 6. <u>HEWLETT-PACKARD JOURNAL</u> "A New Series of Programmable Calculators"
- 7. <u>HEWLETT-PACKARD JOURNAL</u> "9800 Processor Incorporates 8-MHz Microprocessor"
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<u>COMPUTER DESIGN</u> - "Small Computer Features Extensive Software and File-Oriented DOS" -Reprinted with permission from the December 1972 issue of COMPUTER DESIGN.

The first of a planned family of microprogrammed small computers, the PRIME 200 is claimed to be unique in the small computer marketplace in that its software was completely specified before the hardware was designed. Prime Computer, Inc. 17 Strathmore Rd., Natick, Mass., the manufacturer, will provide the computer to customers complete with extensive, fully field-tested software, including a file-oriented disc operating system (DOS) developed at NASA. The design approach was to first develop an integrated software system far more powerful and much easier to use than currently available small computer software and to take advantage of new components and fabrication techniques to result in a hardware capability that would optimize the software performance.

The software package includes a FORTRAN IV compiler, an advanced macro assembler, and a full array of loaders, debugging aids, and utility programs. Many features of the DOS - especially in the area of uniform conventions for handling files - are claimed to be those normally found only on very large data processing machines, essentially "providing system 360-type DOS sophistication in a small computer environment."

MOS semiconductor memory is used exclusively. Memory is packaged on 16 x 18" PC boards with 8K of 16-bit (plus two parity bits) memory on a single board. The entire CPU and the EIA-compatible I/O interface are continued on a single board, minimizing interconnection problems. Memory is expandable to 32K, 16-bit words.

Fully microprogrammed logic is incorporated. The computer features a 64-bit wide microprogrammed word for speed and efficiency within the microprogrammed environment. This technique is called "horizontal microprogramming" and is similar to the technique used on model 370/165 machines. Full cycle time is less than 750 ns, and the processor cycle time is as short as 160 ns. The technique provides for simple, low-cost implementation of such features as floating-point arithmetic, decimal arithmetic, and character and byte edit instructions.

An important extension provided by microprogramming is microdiagnostics, which permits fault diagnosis to the component level over a large portion of the machine. Standard features include parity for performance analysis and error checking on every byte of information, on all data paths and address paths to memory and to all I/O devices. Since there is parity on every byte of every data path within the central processor, if an error does occur, the user will know about it instantly and be able to take appropriate action.

There are no wires within the mainframe. Simplified maintenance is achieved through plug-in packaging. The processor, memory, I/O controllers, power supply, backplane, and control panels are all plug-in units. All of the large-board modules plug into a 10-slot backplane which is itself a plug-in module. This approach makes all modules, including the power supply, readily accessible for easy maintenance. Also, the machine can be extended in the field, such as adding a tape or disc drive.

The basic configuration includes a central processor with a cycle time of 750 ns, 8K-word MOS memory, byte parity, eight DMA channels, asynchronous serial communications interface, programmer's console, 64-level vectored priority interrupt system, and expansion capacity for eight additional circuit boards. The instruction complement includes 124 instructions, 15 of which are memory references for fast, efficient data handling without time-consuming register housekeeping (eg, a register-to-memory add requires only a single word instruction). <u>COMPUTER DESIGN</u> - "Microcomputer Programmable ROMs" - Reprinted with permission from the December 1972 issue of COMPUTER DESIGN.

A0-740,-742, and -743 plug into SIM4-01 or -02 prototyping boards to perform all functions of a FORTRAN IV assembler, eliminating need for a general-purpose computer and enabling an MCS-4 microcomputer prototype to assemble its own programs. The programmable ROMs translate symbolic assembly language into bit patterns suitable for entry into the microcomputer's control ROM. The assembler accepts input source text from a teleprinter on each of two required passes. The first pass creates a name table and source listing; the second rereads the source text and punches tape used to program the control ROM, using MP7-02 programmer and MCB4-10 interconnection chassis in conjunction with the prototype board. Users can assemble the program, generate a programming punched tape, enter the program in control ROMs, and debug the program; then, without hand-wiring they can assemble a complete microcomputer which requires only 5- and -10-V supplies to become fully operative. Intel Corp., Santa Clara, Calif.

<u>COMPUTER DESIGN</u> - 'Microprogrammable Computer/Controller Designed for Dedicated Applications" - Reprinted with permission from the December 1972 issue of COMPUTER DESIGN.

A 16-bit microprogram instruction set with execution time of 200 ns, and over 53 instructions within five instruction classes are standard on the C A S H-8. The computer/controller bridges the gap between chip-level, special-purpose, hardwired controllers and general-purpose minicomputers. Two plug-in cards contain the processor and up to 512 words of TTL ROM. The ROM stores the user's microprogram location in an external memory of up to 65K words in "controller" and "hybrid" modes, or up to 1K general-purpose microinstructions in "computer" mode. The ROM can be expanded by adding cards, it can be replaced by a read/write memory, or a combination of the two memory types can be used for up to 65K directly addressable words. A total of 16 programmable file registers can be used as storage, index values, address modifiers, and shift registers. Other features include an external priority interrupt system, I/O echo, and programmed I/O from any file register or memory. Standard Logic Inc., Santa Ana, Calif.

DATA PRODUCT NEWS - "Low-Cost Commercial Minicomputer" - Reprinted with permission from DATA PRODUCT NEWS, Vol. 4, No. 4

Developed for process control applications.

The BDX-9000 is a new 16-bit parallel-processing computer that is microprogrammable and provides two microseconds add time. The new mini is unusual in that it is functionally interchangeable with a previously developed aerospace computer, the BDX-900, which is used in a number of aerospace applications. These two computers are completely compatible with regard to software and interface, permitting the BDX-9000 to be used during early ground-based evaluation test exercises. This procedure allows the airborne BDX-9000 to be phased in at a later program stage without requiring any changes.

Extensive use of LSI and MSI circuitry provides high performance in a small area; the entire central processor, for example, is contained on one printed circuit card. This facilitiates maintenance, as well as allocating space in the basic chassis for up to 24,576 words of core memory contained on four cards, and 12 peripheral device controllers using three cards. Cards measure 11.5" x 16".

A complete line of add-ons is being developed for the new minicomputer, including a six-microsecond multiply option and a fast fourier transform module, together with an extensive software package. The BDX-9000 is 7" high, 19" wide and 20" deep, including power supply, and weighs 40 pounds.

The Bendix Corporation, Teterboro, New Jersey. (201-288-2000), (Navigation and Control Division) 07608.

<u>BENDIX TECHNICAL JOURNAL</u> - Summer/Autumn 1972 - "Minicomputers in Automatic Test Systems" - T.J. Meloro - Reprinted with permission

This paper discusses the use of minicomputers in automatic test systems. It reviews briefly some of the more recent developments in test-system technology, and discusses the advantages that accrue from computer control. It then examines the requirements that such systems impose on the computer with respect to architecture, word length, speed, memory, input/output, peripherals, and software. Finally, a computer is described that meets the requirements imposed by these parameters.

# Introduction

The emergence of the low-cost, high-performance minicomputer has brought flexible automation to many processes for which the general-purpose digital computer had previously been considered unsuitable. Such is the case with testing equipment. A few years ago, test systems were made up of manually controlled test devices - signal generators, oscilloscopes, multimeters, etc. - applied to the unit under test (UUT) by an operator; today, general-purpose digital computers are used to automate complex test systems containing a variety of sophisticated programmable devices.

Manual test systems for different applications had little in common. Test procedures were individually prepared, with little uniformity in format and content. As a consequence, these systems had limited utility, and costly redesign was required as each new series of test units emerged. The first significant step toward development of a modern automatic test system came with the programmed controller. A major improvement over previous manual systems, the programmed controller employed a predetermined sequence of instructions stored on some medium such as punched paper tape. As it read the tape, test by test, the controller applied appropriate signals to stimulate the UUT and made connection with the proper instrument to measure UUT response. Although not particularly flexible, the programmed controller was automatic in that, once actuated by the operator, it read and executed the entire test program independently. In most systems, the results of unsatisfactory tests were printed out and subjected to subsequent fault analysis.

In essence, the programmed controller was a special-purpose digital computer. Control tapes were written in specially developed test languages, though no standardization of language was ever achieved. This controller has since been superseded for many applications by the computer-controlled test system, the result primarily of the advent of the minicomputer. The minicomputer provides the flexibility and program-storage capability of a general-purpose digital computer at a cost that is almost competitive with that of the programmed controller....

## Architecture

Many design decisions are involved in developing the architecture of the centralprocessor unit of a computer for a particular field of application. Some of the more important of these decisions concern the composition of the instruction set, modes of addressing, type of data flow (parallel or serial), register organization, and controlunit implementation. Because flexibility is the outstanding characteristic of a computer it is rare that a particular architecture is uniquely suited to a particular application. Skillfully applied, different architectures can often do equivalent jobs. In practice, the problem becomes one of selecting the design that will do the job at lowest cost, all factors considered.....

....Control-unit implementation, which concerns the techniques employed in executing individual instructions, may be of two types: hard-wired or microprogrammed. Although the difference means little to the user, it is important to the minicomputer designer. Recent developments in large-scale integration have made microprogramming a costeffective alternative to the more conventional hard-wired technique. For the balance of this article consult the Bendix Technical Journal - Summer/Autumn 1972. <u>HEWLETT-PACKARD JOURNAL</u> - December 1972 - "A New Series of Programmable Calculators" -Richard M. Spangler - Reprinted with permission from the HEWLETT-PACKARD JOURNAL -December 1972.

The three calculators and many peripherals of the 9800 Series are designed to handle the broadest possible range of applications. Flexibility and expandability are emphasized.

In recent years, programmable calculators have taken on a large portion of the computation jobs that were previously handled by computers. Calculators have several advantages that are responsible for this trend. Calculators are small, self-contained, and easily transported - they can be brought directly to the user's desk. They are quiet, and fit easily into a laboratory or office environment. No complicated turn-on procedure is required; the user merely turns on the power switch, and the calculator is ready. The most important advantage is a psychological one - calculators are "friendly". They are interactive, they provide immediate feedback and immediate answers, and they are dedicated to their user.

The 9800 Series is a new line of powerful programmable calculators and an extensive set of calculator peripherals. The series is designed to cover a broad range of applications. Important objectives of the new series are to provide the user with a choice of calculators that are flexible and expandable, and to support those calculators with comprehensive applications software and peripherals.

The new 9800 Series is the successor of the  $9100A/B^1$ , HP's first programmable calculators. These earlier calculators were as powerful as the limits of technology at the time of their conception would allow them to be. But with technological advances come better calculators, hence the 9800 Series.

## Three Models

There are currently three calculators in the 9800 Series. Model 10 is a key-perfunction calculator with a keyboard and language that are extensions of the HP9100A/B. The display is a three-register numeric display like the 9100A/B's, but uses sevensegment light-emitting-diode characters rather than a cathode-ray tube.

Model 20 has a statement-oriented algebraic language. The user doesn't have to position his variables in special registers or keep track or temporary results. He can enter arithmetic expressions in the same order as he would read them, including parentheses. Model 20 even allows implied multiplication, something that's not allowed even in most high-level computer languages. Model 20 has a display of 16 alphanumeric characters that can display a whole statement at a time. The alphanumeric display can be used during program execution to display comments and instructions as well as numeric results. This capability enhances the interactiveness of this model.

Model 30 is even more interactive. The keyboard is alphanumeric, like a typewriter, rather than key-per-function. This complements the 32-character alphanumeric display by making it convenient to enter text and messages. The programming language of the Model 30 is BASIC, a well-known and easy-to-learn computer language that is designed for use in interactive environments.

The electronics of the 9800 Series is general in design and is common to all three calculators. The central processing unit is a microprogrammed, 16 bit serial processor that implements a general computer machine language (see article following this one). The three separate keyboard languages and the arithmetic routines are implemented by firmware routines stored in MOS read-only memory (ROM), and the user's programs are stored in MOS read-write memory. The input/output structure is a general purpose system which makes it possible to interface with a wide variety of peripherals.

# Many Peripherals

Some of the more important peripherals that have been interfaced are:

9860A	Card Reader
9861A	Output Typewriter
9862A	X-Y Plotter
9863A	Mechanical Paper Tape Reader
9864A	Digitizer
9865A	Magnetic Tape Cassette
9866A	Thermal Line Printer
9869A	Hopper Fed Card Reader
2570A	Instrumentation Coupler
2748A	Paper Tape Reader
2895A	Paper Tape Punch

Several general purpose interface cards are also available to interface with other HP instruments, the new HP interface system<sup>2</sup>, and many peripherals from other manufacturers.

# Flexible and Expandable

Flexibility and expandability of the keyboard and programming languages of 9800 Series calculators are provided through the use of add-on ROM modules. From the optional ROMs available, the user can select the language features that are required by his particular discipline.

	9100A/B	9810A	9820A	9830A
Language	Reverse Polish	Reverse Polish	Algebraic	BASIC
Keyboard	Key per function	Key per function	Key per function	Alpha- numeric
ROM size (bytes)	4K	5K to 11K	8K to 14K	15K to 31K
RWM size (bytes) available to user	128(A);256(B)	908 to 2924	1384 to 3432	3520 to 7616
User definable Keys or func- tions	None	Optional - single key subroutine	Optional - single key subroutine or func- tion with parameters	Standard- subrou- tine or function with one parameter
Recording device	Magnetic Card	Card with Cassette optional	Card with Cassette optional	Cassette standard
Display	3 register numeric CRT	3 register numeric LED	16 character alphanumer- ic LED	32 charac- ter alpha- numeric LED
Primary Printer	Optional 18 column numeric	Optional 16 column alpha- numeric	Standard 16 column al- phanumeric	Optional 80 column alphanum <del>-</del> eric

## Comparing 9800 Series Calculators

In Model 10, three ROM blocks of up to 2048 bytes each may be added to the calculator. The first block is used to define and implement the functions of a set of 15 keys on the keyboard. The second and third blocks are for control of internal and external peripherals.

In Model 20, three blocks may be added, each controlling one of three sets of ten keys on the keyboard.

In Model 30, eight blocks may be added, and since the Model 30 has an alphanumeric

keyboard, no special keys are required. The ROMs are accessed through mnemonics which are entered as a sequence of alphabetic characters.

## Different Models for Different Users

Each of the three calculators is general purpose, but each has features which make it more appealing to different sets of users. Model 10's advantages are its low cost, and its compatibility with the 9100A/B, which provides the basis for an extensive applications program library. For example, the Surveying and Statistics applications packages that were originally developed for the 9100A/B have been updated and expanded to make use of the new features of Model 10.

Its natural algebraic language and its many programming and editing features, such as program flags and relative addressing, make Model 20 ideal for users who want to do their own programming. These features are particularly appealing to research scientists and engineers. The peripheral control capabilities of the Model 20 also make it attractive for use as a controller in instrumentation systems<sup>2</sup>.

Its larger memory, its array-variable capability, and its built-in tape cassette make Model 30 appealing to users with large programs and data bases, such as structural engineers and investment analysts. The alphanumeric keyboard, string-variable capability, and page-width printer appeal to users in fields outside the scientific, such as education and business. The programming language of the Model 30 appeals to a large number of users who already know BASIC as a time-sharing language. With an optional Terminal ROM, time-share users can transform the Model 30 into a versatile terminal with local as well as remote computation and storage capability.

With all three calculators, each user can specify a system of optional ROMs, peripherals, and read-write memory size to meet his own needs. This versatility is enhanced by user-definable keys, optional on the Models 10 and 20 and standard on Model 30. All three machines can also be expanded by the use of special machine language programs that can be loaded into read-write memory from a magnetic card or cassette. This capability can be used, for example, to supply a software driver for a special peripheral.

The special features of each calculator along with the general purpose nature of the hardware are designed so that some combination of 9800 Series instruments will provide a solution to almost any programmable calculator application.

# References

- 1. Hewlett-Packard Journal, September 1968.
- G.E. Nelson and D.W. Ricci, "A Practical Interface System for Electronic Instruments," Hewlett-Packard Journal, October 1972.

<u>HEWLETT-PACKARD JOURNAL</u> - December 1972 - "9800 Processor Incorporates 8-MHz Microprocessor" - Reprinted with permission from the HEWLETT-PACKARD JOURNAL December 1972, (The following are excerpts only).

The processing unit for HP 9800-Series calculators is a microprogrammed 16-bit serial processor that is capable of executing 75 basic machine-language instructions. The processor

- . controls the data flow between memory and working registers,
- . performs logical and binary or decimal arithmetic operations on data in the working registers,
- . performs logical decisions (branching) based on the states of 16 qualifiers (carry/borrow, operation codes contained in machine-language instructions, etc.),
- . controls the internal clock for variab-cycle-time microprogram steps, and
- . transfers control to the I/O controller for input and output instruction execution.

The processing unit is implemented with MSI bi-polar logic circuitry with strong emphasis on read-only memories. Central control of the processor, memory, and I/O unit is nested in microprograms stored in these ROMs in the microprocessor action of

the processor. The microprocessor executes machine-language instructions in cycles by following these microprograms.

(For complete article refer to Journal)

<u>COMPUTERWORLD</u> - January 24, 1973 - "Microdata's Dual Processors Designed for Data Networks" - Copyright Computerworld, Newton, Mass. 02160.

IRVINE, Calif. - Microdata's 1600/60 Communications Processor is designed to upgrade the firm's line of communications interfaces and software packages to assemble programmable communications systems.

Each of the 1600/60's two independent CPUs has its own I/O system and microprogram control memory.

One CPU - a general purpose computer - is dedicated to system control, control of peripheral devices and message processing. The second CPU, the COM-60, services up to 256 synchronous and/or asynchronous communications channels operating full- or half-duplex with throughput up to 40K char./sec, the firm's spokesman commented.

Typical applications for the new system might be a data concentrator, front-end preprocessor and store-and-forward message-switcher, a company spokesman said.

Price for a typical system with 64 asynchronous modem interfaces, 32K bytes of core memory and cabinets is \$29,000 from 17481 Red Hill Ave., 92705.

<u>COMPUTERWORLD</u> - March 7, 1973 - "Microprogramming Coming Into Vogue, Costs Seen Dropping" - Copyright Computerworld, Newton, Mass. 02160.

SAN FRANCISCO - Microprogramming has become a highly practical reality through the use of advanced semiconductor technology in control memory design, Microdata President Donald W. Fuller told a group of security analysts recently.

But the full force of the technique, recognized as a theory with great potential 20 years ago, is only beginning to be felt.

### On the Bandwagon

Almost every computer maker has incorporated microprogrammable computers in the product line, he noted. "No wonder, when you realize what microprogramming can do for the user as well as the manufacturer. The cost of developing new computer architectures is the lowest ever," he said.

The manufacturing cost for a family of related models has dropped dramatically as have costs for training and servicing. And with microprogramming, software can be fully protected from theft by the competition," Fuller said.

<u>COMPUTER</u> - "Microdata 1600/60 Communications Processor" - Reprinted with permission from February 1973 issue of COMPUTER.

Microdata Corporation announces the Microdata 1600/60 Communications Processor. According to Director of Marketing - Robert Oakley, the new processor combines dual CPU hardware with full communications handling firmware to achieve excellent cost/performance. The processor, when combined with Microdata's full line of communications interfaces and software packages, allows complete programmable communications systems to be assembled.

Each of the 1600/60's independent CPU's contain separate I/O systems and microprogram control memories. A common main core memory and CPU to CPU interrupt system permits separation of line discipline and character handling with the message processing tasks. Simultaneously, the system maintains complete initialization/completion interaction between the two functional CPU's. One CPU, a general-purpose computer, is dedicated to system control, control of peripheral devices, and message processing. The second CPU, called the Communications Operating Module (COM-60), services up to 256 synchronous and/or asynchronous communications channels operating full or half duplex with throughput up to 40,000 characters per second.

Information tables containing control for individual channels are stored in core memory and accessed by COM-60. The tables provide control of each line with respect to speed, character and message formats, external control codes, and other characteristics.

The 1600/60 is intended for use as a data concentrator, front-end preprocessor, or store-and-forward message switcher, and nearly all related communications system applications. It exceeds the performance requirements for most applications, but is priced low enough to be economically feasible for smaller systems. Price for a typical system with 64 asynchronous modem interfaces (103 or 202), 32K bytes of core memory and cabinets is \$29,000. Contact: Robert Oakley, Microdata, 17481 Red Hill Ave., Irvine, CA. 92705.

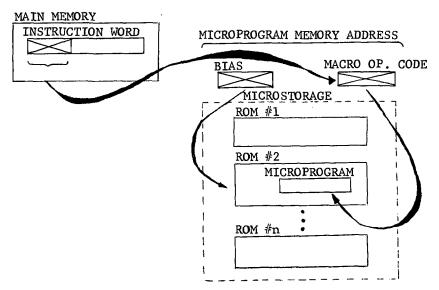
<u>SIGARCH</u> - "On Computer Architecture, Software Portability & Microprogramming" - Reprinted with permission from SIGARCH

Current pressure to lower the cost of software for aerospace systems has increased interest in software portability. Recently, in a discussion concerning architectural features which support such portability, we stumbled upon a concept which appears unique to us and to have considerable merit in the design of future aerospace computers.

The concept is basically this: to use a bias register for addressing multiple microprogrammable memories, each of which contains a complex set of procedures for decoding a mutually exclusive macro-instruction set. This will require a general structure microprogrammable machine. Some of the inherest technical and economic benefits of the concept are:

- (a) Machine independence of major software components. A small pluggable component can be microprogrammed as an adapter without affecting other software already operational on the system.
- (b) An instruction set can be specified concurrent with software specifications for software components which effect functional optimization.
- (c) Tailored system efficiency on diverse computing tasks.
- (d) Fault tolerance -- by implementing the same basic instruction set in various microprogrammable memories, using variant hardware capabilities, high-failure components which provide high-speed capabilities may be backed-up by lowerspeed but otherwise equivalent capabilities. Such alternate implementations could also simplify fault isolation procedures.

As shown in the figure below, the procedure executed for the macro operation code present in an instruction word in main memory would depend on the current value of the microprogrammable memory bias register.



An effective linking approach would be for the executive program to operate in a privileged state with which a specific instruction set would be associated, including the set-ROM-Bias-register-and-transfer-control to a specific software function in the task mode. (The ROM designation would be included as a part of the preamble data for each task.)

At task completion the return-to-executive-state instruction (common to all ROM's used by the tasks) would reset the ROM Bias register to again specify the address of the ROM associated with the privileged state.

Alternatively, authority over the bias register assignment could be at an individual routine/subroutine level. A call/return duplex instruction capability could be incorporated which, in addition to storing and restoring the program counter, would also perform these functions for the ROM bias register. This would immediately open up complete libraries of software functions to even a completely new and unique machine organization.

With read/write microprogrammable memories, a roll-in/roll-out instruction set could be implemented compatible with the roll-in/roll-out software modules, extending the resource nature of instruction sets another level. Perhaps special instructions could be dynamically allocated on an individual case basis depending upon the storage load of the microprogrammable memory. This has direct implication in the case of casualty-reconfiguration operations.

<u>COMPUTER DESIGN</u> - March 1973 - "Ruggedized Minicomputer Meets Mil-Spec Airborne, Shipboard Applications" - Reprinted with permission from COMPUTER DESIGN - March'73 issue.

A 16-bit, general-purpose, severe environment minicomputer, the 1602 Ruggednova features a core memory cycle time of 1 s. An MSI/LSI microprocessor executes 32-bit microinstructions at a 5-MHz rate. At the microprogram level, 25 full-length registers are available. Only one-eighth of the microprogram capacity of 4K words is used to create the extended instruction set. Instructions include double precision and a powerful file search. An interrupt branching and nesting processing capability performs all the preliminary tasks necessary to process an interrupt. The system provides the flexibility of software-vectored interrupts with the speed and ease of a hardware-vectored system. Environmental specifications meet or exceed MIL-E-16400 shipboard, -E-5400 airborne, -461A electromagnetic interference, and -S-901 shock test. Two chassis sizes are available: an ATR short package containing the CPU and 8K of memory, that measures 7 5/8 x 10 1/8 x  $12\frac{1}{2}$ "; and a standard ATR 7 5/8 x 10 1/8 x  $15\frac{1}{2}$ " package that contains five I/O slots. Additional memory can be added to either package by plugging memory modules into the computer chassis. ROLM CORP., Cupertino, Calif.

<u>COMPUTER DESIGN</u> - March 1973 - "Microprogrammed Branch Driver" - Reprinted with permission from COMPUTER DESIGN - March'73 issue.

A 16-bit microprocessor CAMAC branch driver, the MBD-11 can function as a standalone controller for data logging and control applications and as a 8-DMA-channel multiplexer/ branch driver for a PDP-11 series computer. It serves as a preprocessor and parallel processor, has a 16-bit read-write bipolar memory that is expandable to 1024 words in 256 -word increments, and has 16 microinstructions that can select any memory source, transfer to any register, and perform 1 of 16 control functions in 350 ns. The unit can initiate 25 unique interrupts to the PDP-11. BiRa SYSTEMS, Inc., Albuquerque, NM.

<u>COMPUTERWORLD</u> - March 28, 1973 - "HP Unveils 'Top-of-Line' Mini With Writable Control Store" - Copyright, Computerworld, Newton, Mass. 02160.

CUPERTINO, Calif. - Hewlett-Packard has introduced the 2100S Microprogrammable Systems Computer as the top-of-the-line in its minicomputer series.

The basis of the system is the use of a Writable Control Store (WCS) enabling users to write their own instruction sets.

Users can store 256, 24-bit microinstructions on each of three WCS cards.

In conjunction with these cards users can have their own libraries of microprograms on disk. These programs can be transferred to the WCS cards as needed. After execution, the microcoding can be swapped with other microprograms on the disk, or left on the cards

In this manner the user can alter the 2100 at any time, configuring for different functions - e.g., one time as a process control unit, the next as a communications processor.

Users wishing to retain microcode permanently in the central processor can have the instructions fused on Read Only Memory Chips by a feature called the Prom Writer.

This Programmable Read Only Memory Writer consists of one card temporarily inserted into a 2100S I/O slot and a small box in which the ROM chips are fused.

Software provided with the Prom unit enables the system operator to control the fusing with chips automatically verified and any missing bit re-fused.

The basic 2100S comes with a complement of 102 microinstructions and 86 basic machine language instructions.

The central processor has a cycle time of 196 nsec.

Basic configuration includes a 16K-word memory, communications control channel, hardware floating point, crystal-controlled time base, two software assignable direct memory access channels, memory protect, memory parity, power fail and extended arithmetic instructions.

The 2100S sells for \$16,000 and is available on a lease or rental basis. First deliveries are set for mid-1973.

<u>COMPUTERWORLD</u> - March 21, 1973 - "Mini Allows Users to Write Own Instruction Set" - Copyright Computerworld, Newton, Mass. 02160.

OCEANPORT, N.J. - A new computer from Interdata incorporates a user-alterable Dynamic Control Store (DCS) which allows the user to write his own instruction sets, special algorithms or application functions.

The Interdata Model 85 is a 16-bit computer with an interleaved MOS/LSI solidstate memory providing a 270 nsec average main memory cycle time.

Capacity is 16K bytes expandable to 64K bytes. Standard features include 16 general registers, 15 of which can be used with index registers; hardware multiply and divide and floating point; direct addressing; 255 I/O interrupts with automatic service routine and 131 user level instructions.

The DCS contains 1,024, 32-bit words of 60 nsec bipolar read-write memory that can be used to produce instructions extending the general purpose instruction set.

Later, these user-written instructions can be modified cynamically without hardware modifications. Instructions are entered in much the same way as standard code - from paper tape, console keyboard, etc.

# Standard Software the Same

All existing Interdata and customer software programs now being used on any of the company's New Series processor may also be used with the Model 85.

This includes the standard Interdata Operating Systems: Basic Operating System (BOSS), Disk Operating System (DOS) and a Real-Time Operating System (RTOS).

Additionally, there are two software packages for direct support of the Dynamic Control Store: Microassembler and Microloader/debug programs.

With these programs no simulator is required since routines can be checked out through the DCS and debugged without hardware modifications of any kind, a spokesman said.

Microprograms in the Model 85 are typically three to 10 times faster than user level software for the same function, the spokesman asserted.

Options for the basic Model 85 include memory parity, memory protect, power fail/ auto restart, and a line of peripherals and special modules including dual cassette and a 4,000-channel digital I/O multiplexer.

The Interdata Model 85 will be available in June, 1973. With 16K bytes of memory, built-in teletype interface and DCS, the unit will carry a price tag of \$22,800.

The firm is at 2 crescent Place, 07757.