1600/60 System

Data Communication System

GENERAL DESCRIPTION

The Microdata 1600/60 is a complete data communications system, providing unusual price/performance advantages in communications applications such as data concentrators, communications preprocessors, message switchers, and store-and-forward communications systems.

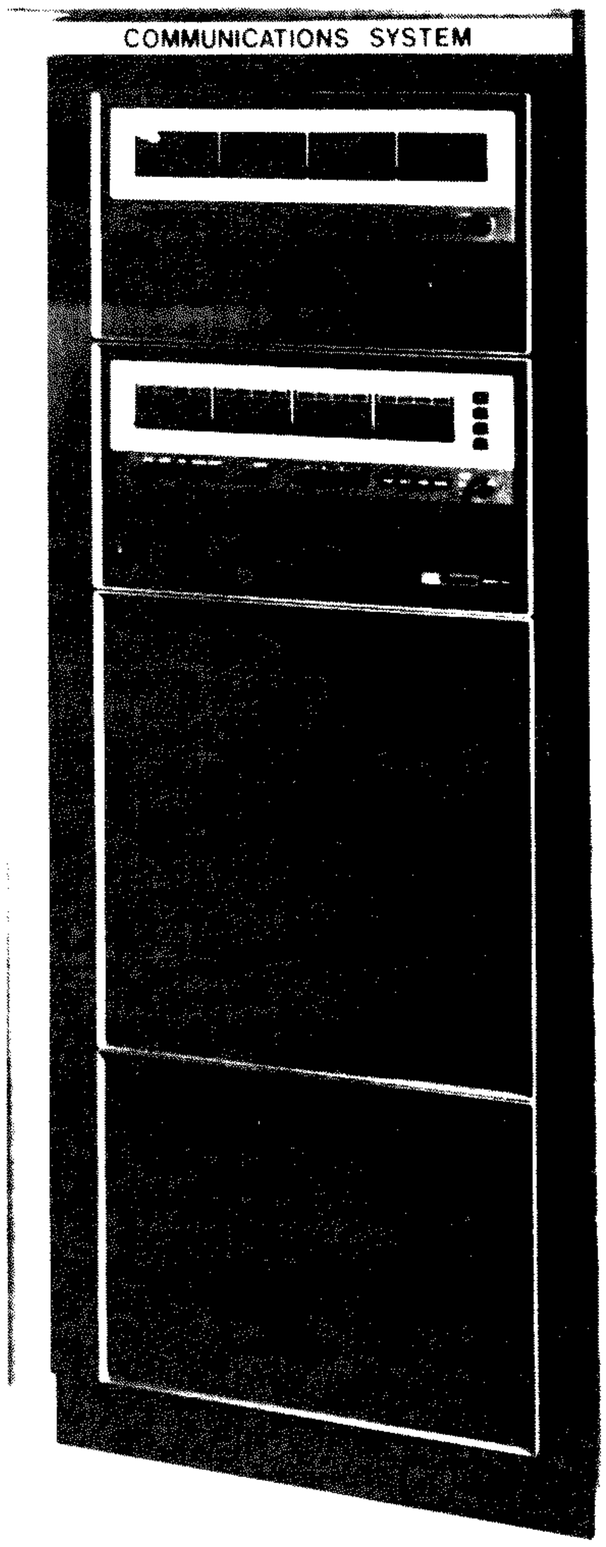

FIGURE 1. 1600/60
DATA COMMUNICATIONS SYSTEM

The unusual efficiency of the Micro 1600/60 system derives from a unique system architecture using two Micro 1600 series processors sharing a single memory, plus specially developed firmware. The firmware has been developed for maximum throughput in a dual-CPU configuration, with one processor equipped with a set of firmware that is oriented specifically to communication line handling tasks, and a second processor equipped with a set of general-purpose firmware that is oriented to character/string handling and storage/retrieval activity.

The dual-CPU configuration with special firmware is augmented by Microdata's standard line of peripheral equipment, plus Microdata's standard line of Communication Controllers and Modem Interfaces. Microdata's communications interfaces provide synchronous, asynchronous, and parallel data communication (including Auto-Call control), and have as standard features; programmable code structures, programmable baud rates, automatic error detection, automatic synchronization, double-buffered input and output, line turn-around control, and multiple modes of I/O operation.

The modular nature of the 1600/60, in terms of memory size and expandable I/O capabilities, enables the user to create a configuration with a cost and performance exactly matching the data communication requirements of his system.

The powerful instruction sets of the 1600/60 minimize the amount of coding necessary to create the communications program, and Microdata programming aids simplify program debugging.

SYSTEM ARCHITECTURE

The computer used in the 1600/60 is the dual-processor Micro 1600D. It incorporates two independent Micro 1600 CPU elements with separate microprogram control memories, and a common main core memory shared by the two processors. This organization permits separation of the communication handling and data processing tasks while maintaining complete interaction between processors.

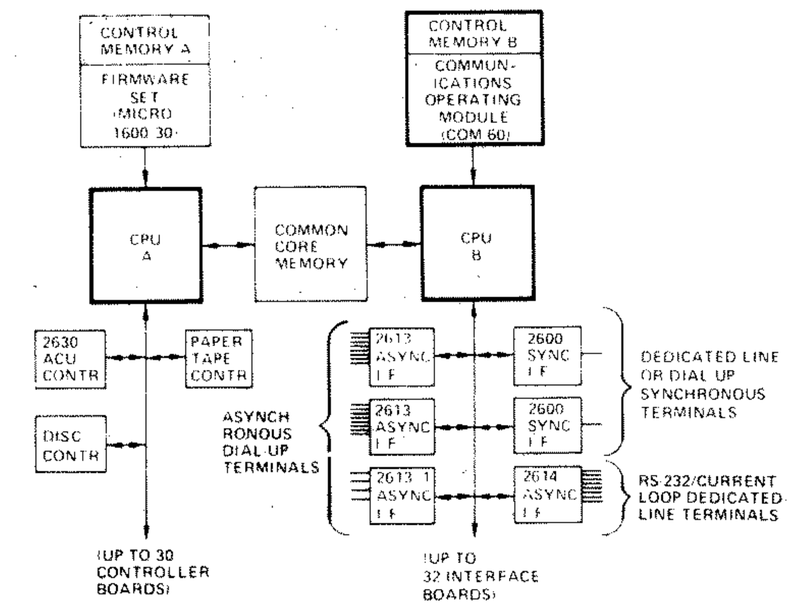

FIGURE 2. 1600/60 FUNCTIONAL DIAGRAM

The first CPU (CPU A) is essentially a general-purpose Micro 1600 processor equipped with a Model 1600/30 control memory. It is intended primarily for central message processing, and for control of system peripheral devices. Communications interfaces may also be connected to the CPU A I/O bus, and controlled by the user's macro program.

The second CPU (CPU B) is also a Micro 1600 processor. However, its control memory is a special set of firmware referred to as the Communications Operating Module (COM–60.) The COM–60, operating at much higher speeds than conventional macro level programs, automatically services up to 256 synchronous and/or asynchronous communications channels operating full or half duplex. Tables containing communication line-control information for the individual channels are stored in the common core memory along with character translation tables. The tables provide fully independent control of each line with respect to line speed, character and message formats, external control codes, and other terminal characteristics.

Although the two CPUs operate independently for maximum efficiency, they communicate freely with one another. Data and control information to or from the communications channels are transferred between CPU A and CPU B via the common core memory. A bidirectional interrupt link is also provided to allow each CPU to interrupt the other.

STANDARD SYSTEM FEATURES

Dual-Processor Task Sharing

The 1600/60 system architecture provides an efficient allocation of line-control and message-management tasks between the two processors and their specialized firmware.

- A bidirectional interrupt link is provided between the CPUs.
- COM–60 operating parameters, held in CPU B file registers, can be changed by CPU A.
- CPU A can control devices on CPU B I/O bus.
- CPU A can direct CPU B execution of microcode.
- CPU B can execute microcode from core memory.

Over 256 Full-Duplex Lines

- The Communications Operating Module (COM–60) in CPU B firmware, services up to 256 synchronous/ asynchronous channels in true full duplex operation.
- The user program in CPU A can service additional communications channels connected to CPU A.

Over 40,000 Character/Second Throughput Potential

The complete character-handling time required by COM–60 is 15 to 25 microseconds, providing an inherent bandwidth in excess of 40,000 characters per second.

Efficient Code Translation

- COM–60 provides automatic character translation.
- Code translation tables in core used by COM–60 in CPU B can be changed *on the fly* by CPU A.
- COM–60 includes extensive Delete Character and other automatic message editing features.

Error Recovery Provisions

- COM–60 automatically restarts in the event of a disabling system error.

Line Control Aids

- Baud rates and transmission formats are programmable on an individual line basis.
- A timer is available for each line, selectable from 1 millisecond to 65 seconds.
- Control codes are detected, and servicing begins automatically.

Line Priorities Assigned Dynamically

- Interrupts from individual lines or blocks of lines can be disabled and armed under program control.
- Lines are serviced on an interrupt basis with priority assigned to each input and output line.

Modularity and Expandability

Minimum Microdata systems can be created with cost and performance matched to a specific application. When system requirements expand, Microdata memory, peripherals, and communication interfaces can be added on a modular basis.

APPLICATION INFORMATION

A few of the many applications of the Micro 1600/60 include data concentration, communication preprocessing, and store-and-forward message switching. These examples illustrate the efficiency of the 1600/60 in most data communications applications.

Data Concentrator

The primary purpose of a data concentrator is to reduce the cost of communication lines when many low-speed terminals connect to a single remote terminal or large computer. Data communications between the local and remote terminals are *concentrated* and transmitted over a single medium-speed long distance line instead of over many low-speed lines.

When a concentrator is programmable, as is the Micro 1600/60, it can provide added savings by reducing the communications overhead in the remote terminal/processor. Overhead-reducing functions performed by the Micro 1600/60 in this application include:

- Character-to-message assembly/disassembly
- Control of multiple communications channels
- Message buffering and transmission speed conversion
- Transmission code conversion
- Error checking and control
- Automatic answering and dialing
- Automatic terminal identification

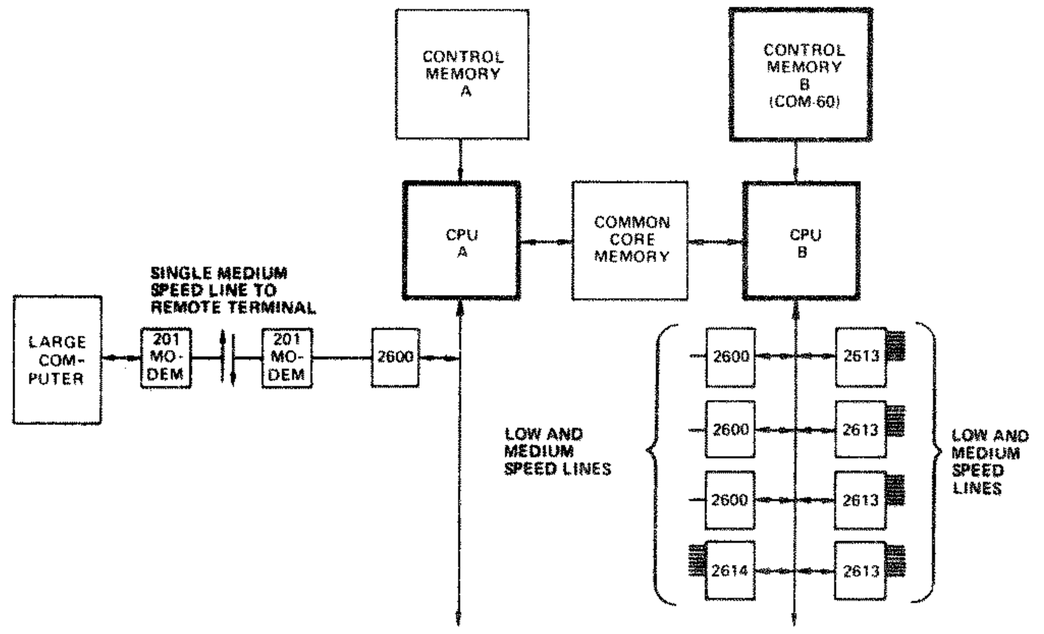

FIGURE 3. 1600/60 DATA CONCENTRATOR

Communications Preprocessor

As an alternative to hard-wired communications controllers and transmission control units in a large computer system, a communications preprocessor can perform all the functions of the controllers plus many valuable added operations which improve system performance and decrease costs.

The Micro 1600/60 used as a communications preprocessor can manage large numbers of low- and medium-speed terminals (such as Teletypes and CRTs) as well as distant terminal controllers and data concentrators. In addition to the functions described for the data concentrator application, the Micro 1600/60 can perform preliminary processing operations which save time on the large computer.

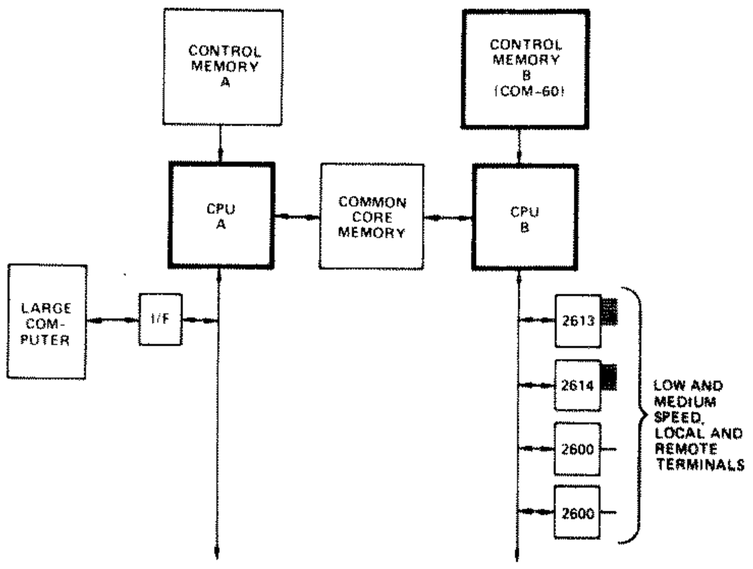

FIGURE 4. 1600/60
COMMUNICATIONS PREPROCESSOR

Store and Forward Message Switcher

This application uses the Micro 1600/60 equipped with a mass storage device (such as a disc) to receive and store messages from a number of data terminals for later transmission to destination terminal(s) or large computer systems. Any terminal can originate a message and transmit it to the central Microdata system. Here messages are stored until they can be forwarded to the destination. Any terminal can address a message to any other terminal without restriction due to differences in line speeds or transmission and control characteristics. The Micro 1600/60 performs all necessary conversions.

Functions performed by a store and forward message switcher typically include the following:

- Polling and addressing terminals
- Message assembly/disassembly
- Message type and destination analysis
- Message re-formatting
- Time and data identification of messages
- Message management in storage
- Message stacking and sequenced transmission
- Code and speed conversion
- Message routing
- Line control
- Error detection and control

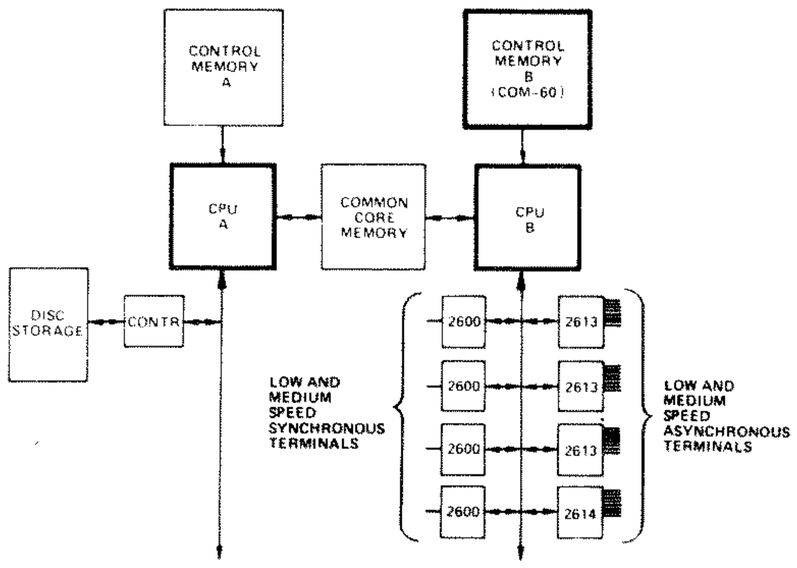

FIGURE 5. 1600/60
STORE AND FORWARD MESSAGE SWITCHER

FUNCTIONAL DESCRIPTION

As shown in the system functional block diagram (Figure 2), the main elements of the Micro 1600/60 data communications system are; two central processor units, two read-only control memories, common main core memory, and the external interfaces.

Central Processor Units

The two central processor units are standard Micro 1600 CPU elements. In conjunction with the other system components, each is an independent microprogrammable computer containing its own control section, arithmetic/logic section, input/output system, and full array of registers.

Each Micro 1600 CPU processor is ideally suited to communications uses. Its 8-bit, byte-oriented operation is matched to the transmission characteristics of communications devices. The Micro 1600 executes micro instructions from 200-nanosecond read-only memory and macro instructions from 1-microsecond core memory. In addition, the powerful macro and micro level instruction sets, the I/O system with high-speed DMA capability, a real-time clock, and a full complement of operational registers provide a high degree of power and flexibility in the data manipulations encountered when dealing concurrently with a large number of I/O channels.

Primarily, CPU operation is controlled by microcommands stored in control memory. This microprogram (firmware) generates the control and timing signals which govern all CPU activities. A Micro 1600 CPU can be applied directly to problem solutions by full programming at the micro level. This is the case with CPU B which executes the COM–60 microprogram directly from control memory. The CPU A firmware, however, causes its processor to fetch and execute macro level instructions written by the user and stored in core memory. Thus, while CPU B operates at high speed from a relatively fixed program, CPU A retains full programming flexibility for each individual system.

Core Memory

The core memory, shared by both CPUs, consists of 4096- or 8192-byte plug-in modules with 8-bit word length, 1.0-microsecond full cycle time, and 400-nanosecond effective access time. In the Micro 1600/60 system, minimum memory size is 8192 bytes, modularly expandable to 65,536 bytes for more sophisticated configurations.

Control Memories

The microprogram control memory for each CPU is a high-speed semiconductor read-only memory with a full cycle time of 200 nanaoseconds. Sixteen-bit micro instructions are fetched and decoded by the CPU control section to determine the actions of the processor, the core memory, and the input/output system. The Micro 1600/30 control memory used with CPU A interprets macro instructions stored by the user in core memory. The Communications Operating Module for CPU B is fully implemented in control memory, and references core only when referring to control tables or when reading or storing data.

Input/Output Systems

Each CPU has its own separate input/output system consisting of data input lines, data output lines, and I/O control lines. These lines are available on the main chassis backplane, and are extendable to expansion chassis backplanes, for connection with I/O interfaces and controllers.

Input/output operations are controlled by the Micro 1600/60

microprograms. The CPU A firmware is designed for macro level programmed and concurrent I/O operations with all standard Micro 1600 peripheral controllers and I/O interfaces. The special-purpose COM–60 firmware in the CPU B control memory provides automatic high-speed scanning and servicing of synchronous and asynchronous communications interfaces.

Additionally, a direct memory access (DMA) port which allows externally controlled transfer directly with core memory can be implemented on the CPU A side of the system. The DMA capability permits transfer up to one million bytes per second and is normally employed for high-speed peripherals such as rotating disc memories.

COMMUNICATIONS INTERFACES

Interfaces and controllers for synchronous and asynchronous communications channels and general-purpose peripheral devices are available for the Micro 1600/60 system. All communication interfaces provide half duplex, echoplex, and true full duplex operation with either CPU.

Because of the specialized nature of the COM–60 firmware, only communications interfaces may be connected to the CPU B I/O system. Up to 32 interface boards can be addressed by CPU B for communication with up to 256 asynchronous channels, up to 32 synchronous channels, or combinations of both. General-purpose peripheral controllers for devices such as paper tape equipment and mass memory devices can be installed on the CPU A I/O bus. If desired, communications interfaces can also be connected to CPU A.

Model 2613 Asynchronous Modem Interface

Dial-up or leased-line asynchronous modems are connected to the communications system using the Asynchronous Modem Interface, Model 2613. Each Model 2613 plug-in circuit board can accommodate eight modems. The Asynchronous Modem Interface is also available in an operationally identical four-channel version, Model 2613-1. Baud rate and transmission format are fully and independently programmable for each line, allowing transmission to and reception from a wide range of remote terminals. Transmission format can contain 1 or 2 stop bits, 5, 6, 7 or 8 character bits, and odd, even, or inhibited parity. Baud rate is selected from the following standard rates:

110	Baud	1200	Baud
134.5	Baud	1800	Baud
150	Baud	2400	Baud
300	Baud	4800	Baud
600	Baud	9600	Baud

Model 2614 Asynchronous Communications Interface

Asynchronous terminals such as local CRTs and teletypewriters that use current-loop transmission, and distant terminals that operate over dedicated-line modems are interfaced using the eight-channel Asynchronous Communications Interface, Model 2614. A four-channel version, Model 2614-1, is also available.

Model 2614 can operate with a variety of transmission formats and data rates. However, since this interface is designed for local current-loop devices and for dedicated communication lines, program selectability of these features is not needed. Thus, for economy, the baud rates and formats are selected for each line using jumper wires and switches on the interface board.

Model 2614 will operate in the following combinations of formats and data rates:

		Interface Signal Type	
Baud Rate	Bits Per Character	Current Loop	RS-232-C
75	8	X	X
110	11	X	X
134.5	9	X	X
150	10	X	X
300	10		X
600	10		X
1200	10		X
2400	10		X
4800	10		X
9600	10		X

Model 2600 Synchronous Model Interface

Synchronous terminals are interfaced to the communications system using Model 2600 Synchronous Modem Interface. Each controller provides complete control of one modem operating at any speed up to 9600 baud. By positioning jumper wires on the controller board, the user can choose character lengths of 5, 6, 7 or 8 bits, allowing a Synchronous Modem Interface to service a variety of terminal types. Synchronization with the remote terminal is performed automatically in the 2600 after the program once defines the synch character. Additionally, the capability for automatic answering of incoming calls is provided.

Model 2630 Automatic Call Unit Controller

Automatic dialing of synchronous and asychronous communications chahnels connected to either CPU can be accomplished using Bell type 801 Automatic Call Units and Microdata Model 2630 ACU controller. Model 2630 is installed on the CPU A I/O system and is operated by the CPU A program. Each controller can accommodate up to four ACUs.

PERIPHERALS AND CONTROLLERS

The complete line of Micro 1600 peripheral devices and controllers can be used to augment the Micro 1600/60 communications system. These peripheral controllers are installed on the CPU A I/O system and are operated by the CPU A program. The DMA capability of CPU A is utulized by high-speed devices.

COMMUNICATIONS OPERATING MODULE

The Communications Operating Module (COM–60) is the microprogram which is actually the heart of the Micro 1600/60 communications system. COM–60 runs independently in CPU B, but is at all times subject to control from the user executive program in CPU A.

COM/CPU A Interaction

The CPU A executive program and the Communications Operating Module communicate via a set of tables in the common core memory and over a bidirectional interrupt link.

The executive program has full control over the parameters of COM–60 operation. When the system is started,

the executive initializes core for the Interrupt Vectors, Inter-CPU Communication Region, Master Reset Parameters, and Terminal Control Tables (TCT). It loads the Master Reset Parameters into the CPU B file registers and starts execution of COM–60. CPU A can continue execution until an interrupt from CPU B specifies CPU A processing. CPU A then processes interrupts from CPU B on a demand basis. All operational parameters are subject to change at any time during system operation. COM–60 operates independently, servicing all communication channels with received data and checking regularly for CPU A interrupts for messages to be transmitted.

Message Reception

COM–60 stores received data in message buffer areas in core. When a complete message is received, COM–60 interrupts and notifies CPU A. The user program can then perform any required message processing.

Message Transmission

CPU A interrupts COM–60 and sets parameters in the appropriate Terminal Control Table (TCT) to affect a message transmission. COM–60 then outputs the message from the core message buffer over the specified channel.

Inter-CPU Interruption

Either CPU can interrupt the other at anytime via the bidirectional interrupt link. When CPU A interrupts COM–60, the interrupt is serviced within 25 microseconds. However, because COM–60 is faster than the CPU A macroprogram, interrupts from CPU B can occur faster than they can be answered by CPU A. Therefore, COM–60 interrupts are queued in two *first-in, first-out* cyclic buffers. The two cyclic buffers are designated high and low priority, and an interrupt from a line can be placed in either buffer as specified in the TCT. The interrupt line from CPU B remains true until the interrupt buffers are empty.

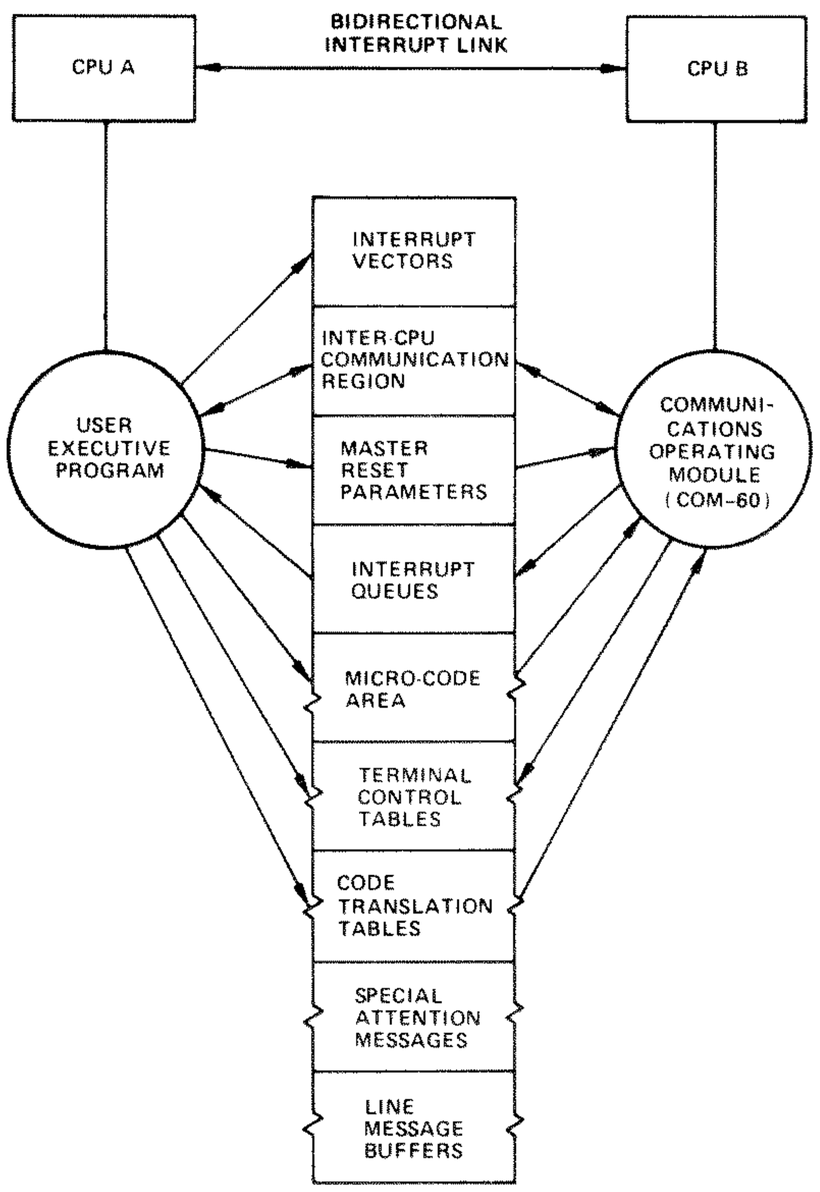

FIGURE 6. 1600/60
INTER-CPU COMMUNICATION

Control Code Handling

Since all lines can operate in the full duplex mode, a remote terminal can transmit a control code at any time. COM–60 checks each character as it is received and takes the appropriate action when a control character is detected. Sixteen *canned* actions for each line reside in firmware, and can be handled exclusively by COM–60 without disturbing CPU A. For other actions, COM–60 interrupts CPU A, and CPU A designates the action to be taken. Single and/or double control character detection is permitted.

Code Translation

COM–60 can translate characters as they are received or transmitted from any 8-bit code to any other 8-bit code by referencing Code Translation Tables in core memory.

PACKAGING

Elements of the Micro 1600/60 Data Communications System are constructed on modular printed circuit boards. The two CPUs, control memories, core memory and a number of I/O interfaces and controllers plug into a 10.5-inch-high mainframe chassis, with additional interfaces and controllers installed in one or more identical expansion chassis. An operator's control panel for CPU A mounts on the front of the mainframe chassis.

As shown in Figure 7, the mainframe and expansion chassis mount on a 63-inch-high standard equipment cabinet. Space in the cabinet which is not occupied by Microdata equipment can be used for peripheral devices and modems. For ease of maintenance, and removal and installation, the cabinet is equipped with two swing-out side doors and a rear door.

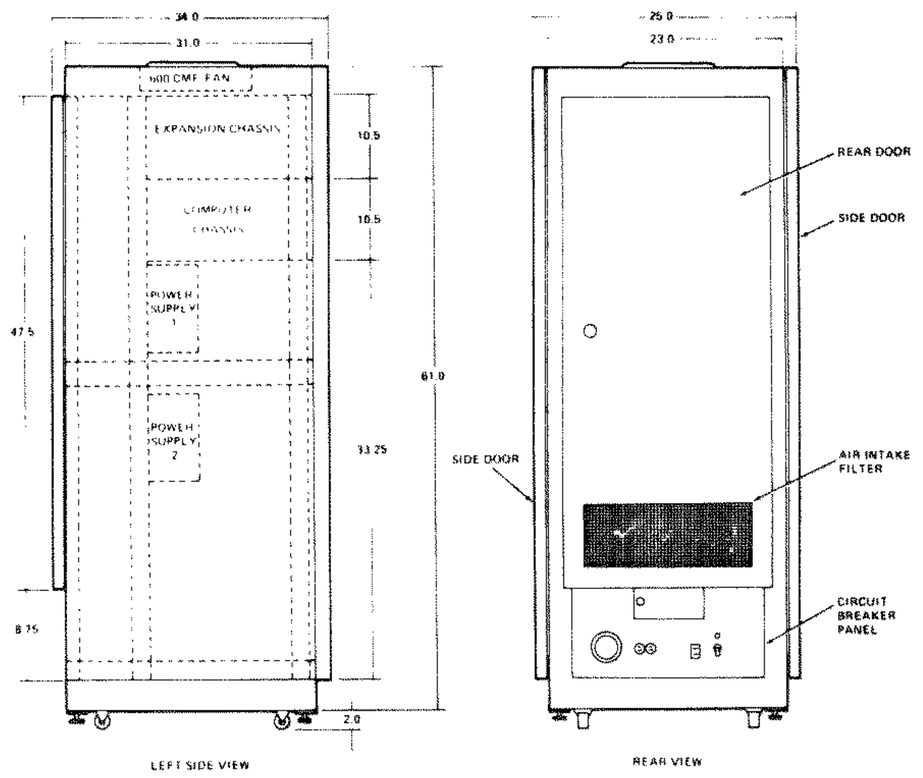

FIGURE 7. 1600/60
INSTALLATION

SPECIFICATIONS

System Organization	Dual-processor organization with CPU A intended for peripheral control and CPU B dedicated to firmware control of communications interfaces.
Central Processor Units	Two Micro 1600 microprogrammable CPUs
Core Memory	Common core memory shared by both CPUs; expandable from 8192 to 65,536 bytes in 4K and 8K increments. 1.0 microsecond full cycle time; 400 nanoseconds effective access time.
Word Length	CPU A Variable—8, 16, 24 and 32 bits; core memory and CPU B—8 bits.
Control Memory:	
CPU A	Micro 1600/30 firmware set
CPU B	COM-60 Communications Operating Module
Communications Operating Module	Special-purpose communications firmware; provides control of up to 256 synchronous/asynchronous communication channels, control code detection/servicing, code translation, plus many other features.
Communications Channels	Synchronous and asynchronous, RS-232-C or 20 milliampere current loop, full duplex operation, selectable formats, selectable speeds up to 9600 baud per line.
Bandwidth	40,000 characters per second for CPU B
Character Servicing Time	Less than 25 microseconds (15 microseconds typical)
Power Supply	19 inches wide, 12.5 inches high, 7 inches deep; mounts in rear of equipment cabinet. Output capacity: +5 Vdc @ 40A, -16.75 Vdc @ 5A +12 Vdc @ 5A
Operating Environment	0° to 50°C, 10% to 90% relative humidity (without condensation)

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